



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/876,301	06/06/2001	Daniel Schoch	231008-0352	9521

7590 01/12/2005

Ted R. Rittmaster  
Foley & Lardner  
Suite 3500  
2029 Century Park East  
Los Angeles, CA 90067-3021

EXAMINER

HUYNH, KIM T

ART UNIT

PAPER NUMBER

2112

DATE MAILED: 01/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/876,301

Applicant(s)

SCHOCH ET AL.

Examiner

Kim T. Huynh

Art Unit

2112

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 08 October 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-31 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-31 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 06 June 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

**DETAILED ACTION**

***Claim Rejections - 35 USC § 112***

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1-10 and 25-31 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The added material which is not supported by the original disclosure is as follows:  
  
Applicant replaced incrementing with modifying. As applicant notes in the specification [0020] discloses the address data is provided to the output generator logic which increments the stored address value and provides the incremented address data to the output. Increments address value is different than modifies address data. Incrementing address means just counting/adding simultaneously as Andreas discloses A0, A1, A2 as in figure 3 whereas modifying address as amended which can be changeable or adjustable. Thus it introduces new matter into the disclosure.  
  
Applicant is required to cancel the new matter in the reply to this Office Action.

***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 11-24 are rejected under 35 U.S.C. 102(e) as being anticipated by  
Andreas (Pub. No US20040093450)

As per claim 11, Andreas discloses an electronic device comprising:

- A controller; [fig.1, 110], [0025]
- A plurality of integrated circuits (lcs) addressable by the controller;  
and[0021-0022], (fig.2)
- A shared bus joining the controller and the plurality of integrated  
circuits;[0021-0022]
- Wherein the controller is programmed to produce a series of addresses on  
the shared bus and to produce an enable signal on an output in  
conjunction with a first address of the series of addresses, [0023-0026]
- Wherein each of the lcs comprises an input for receiving an enable signal  
and an output for providing an enable signal in conjunction with a change  
in address data on the shared bus, and means for storing an address

present on the shared bus as an address of the IC in response to receiving an enable signal, and [0026-31]

- Wherein the input of a first IC communicates with the output of the controller and the inputs of succeeding ICs communicate with the outputs of preceding ICs in a daisy chain configuration. [0025-0027]

As per claim 12, Andreas discloses wherein each of said ICs further comprises a first logic circuit for storing an address present on the shared bus as an address of the IC upon receipt of an enable signal.[0040]

As per claim 13, Andreas discloses wherein each of said ICs further comprises a second logic circuit for generating an enable signal in conjunction with a change in address data on the shared bus.[0026-0031]

As per claim 14, Andreas discloses wherein said second logic circuit comprises a timer that is initialized upon receipt of an input enable signal, and that generates an output enable signal after a period of time that coincides with a rate of address data on shared bus.[0035-0039]

As per claim 15, Andreas discloses wherein said second logic circuit produces an output enable signal upon detecting a first change in address data on the shared bus after receiving an input enable signal. [0026-0031]

As per claim 16, Andreas discloses wherein each of said lcs comprises a processor programmed to initialize a timer upon receipt of an enable signal, and generate an enable signal upon expiration of the timer. [0035-0039]

As per claim 17, Andreas discloses wherein each of said lcs comprises a processor programmed to receive an enable signal at the input, store address data present on the shared bus as the address of the IC in response to the enable signal, detect a change in the address data on the shared bus, and generate an enable signal at the output in response to the change in the address data. [0026-0031]

As per claim 18, Andreas discloses wherein each of said lcs comprises:

- Means for receiving an enable signal at the input; and [0040-0042]
- Means for generating an enable signal at the output in conjunction with the change in the address data. [0026-0031]

As per claim 19, Andreas discloses the electronic device further comprising a storage medium in communication with the controller and having stored therein programming instructions for instructing the controller to produce a series of addresses on the shared bus and to produce an enable signal on an output in conjunction with a first address of the series of addresses. [0037-0041]

As per claims 20, 21, Andreas discloses an electronic device comprising:

- Means for generating an enable signal at an output of a controller and generating first address data on a shared bus; [0021-0022], [0040]
- Means for receiving the enable signal generated at the output of the controller at an input of a first IC; [0026-0031]
- Means for receiving the first address data at a shared bus input of the first IC; [0021-0022]
- Means for storing the first address data in an address register of the first IC upon coincidence of the enable signal and the first address data; and [0035-0037]
- Means for providing an enable signal at an output of the first IC to an input of a second IC in conjunction with a change in address data on the shared bus. [0026-0031]

As per claim 22, Andreas discloses a method further comprising:

- Receiving the enable signal provided at the output of the first IC at the input of a second IC; [0035-0037]
- Storing a second address data present on the shared bus in an address register of the second IC; and [0026-0031]
- Generating an enable signal at an output of the second IC in conjunction with a change in address data present on the shared bus. [0026-0031]

As per claim 23, Andreas wherein generating the enable signal at the output of the first IC comprises initializing a timer upon receipt of the enable signal at the input of the first IC, and generating the enable signal at the output upon expiration of the timer. [0035-0039]

As per claim 24, Andreas discloses wherein the enable signal is generated at the output of the first IC upon detection of a change in address data after receiving an enable signal at the input of the first IC. [0035-0039]

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 1-10 and 25-31 rejected under 35 U.S.C. 103(a) as being unpatentable over Andreas (Pub. No US20040093450) in view of Floyd et al. (US Patent 6,529,979)

As per claim 1, Andreas discloses an electronic device comprising:

- A controller programmed to produce first address data on an output thereof;[0021-0022]
- A plurality of integrated circuits(ICs) addressable by the controller; and [0021-0022], fig.2



- A shared bus joining the controller and the plurality of lcs;([0021-0022], wherein SLICs implies lcs.)
- Wherein each of the lcs comprises an input for receiving address data representing an address of the IC on the shared bus, and an output for providing address data, and [0023-0026]
- Wherein the input of a first IC communicates with output of the controller and the inputs of succeeding lcs communicate with the outputs of preceding lcs in a daisy chain configuration. [0025-0027]

Andreas discloses all the limitations as above except modified address data different from the received address data. However, Floyd discloses the address packet modified in a variety of different manners to provide an indication of a positive acknowledgment, such as modifying other bits, adding other bits, or otherwise modifying the format of the address packet on the return path to the originator of the address packet. (col.8, lines 20-40)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Floyd's teaching into Andreas's system so as to have the advantages to improve communication system and protocol for dedicated configuration to minimizes the amount of circuitry and wire congestion. (col.2, lines 1-5)

As per claim 2, the combination of Andreas and Floyd disclose wherein each of the lcs further comprises a processor programmed to receive address data at the

input, store the address data as the address of the IC, the modified address data, and provide the modified address data at the output.[0031-0036], [0041]

As per claim 3, the combination of Andreas and Floyd disclose wherein each of the lcs further comprises an address register for storing address data received at its input, and output generator logic for modifying the address data.[0031-0036], [0041]

As per claim 4, the combination of Andreas and Floyd disclose wherein each of the lcs further comprises means for receiving address data at the input, storing the address data as the address of the IC, modifying the address data, and providing the modified address data at the output. [0031-0036], [0041]

As per claim 5, the combination of Andreas and Floyd disclose wherein the address data comprises a binary word(fig.1, 182), [0025]

As per claim 6, the combination of Andreas and Floyd disclose wherein the address data comprises a series of pulses representing an address value. [0039]

As per claim 7, the combination of Andreas and Floyd disclose the electronic device further comprising a storage medium in communication with the controller

and having stored therein programming instructions for instructing the controller to produce first address data on the output thereof.[0025-0026], [0031-0036]

As per claims 8, 9, the combination of Andreas and Floyd disclose an electronic device comprising:

- Means for generating first address data at an output of a controller;[0021-0022]
- Means for receiving the first address data at an input of a first IC; [0021-0022]
- Means for storing the first address data in the first IC as an address of the first IC;[0021-0023]
- Means the first address data in the first IC to produce first address data; and[0024-0026], [0031-0036]
- Means for providing the first address data to a second IC through an output of the first IC. [0031-0036]

Andreas discloses all the limitations as above except modified address data different from the received address data. However, Floyd discloses the address packet modified in a variety of different manners to provide an indication of a positive acknowledgment, such as modifying other bits, adding other bits, or otherwise modifying the format of the address packet on the return path to the originator of the address packet. (col.8, lines 20-40)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Floyd's teaching into Andreas's system so as to have the advantages to improve communication system and protocol for dedicated configuration to minimizes the amount of circuitry and wire congestion. (col.2, lines 1-5)

As per claim 10, the combination of Andreas and Floyd disclose the method for initializing further comprising:

- Receiving the first modified address data at an input of a second IC.[0031-0036]
- Storing the first modified address data in an address register of the second IC; [0031-0036]
- Modifying the first modified address data in the second IC to produce second modified address data; and [0031-0036]
- Providing the second modified address data at an output of the second IC.[0031-0036]

As per claim 25, the combination of Andreas and Floyd disclose wherein the modified address data is incremented address data. [0031-0036]

As per claim 26, the combination of Andreas and Floyd disclose wherein the address data is modified by incrementing the address data. [0031-0036]

As per claim 27, the combination of Andreas and Floyd disclose wherein the output generator logic modified the address data by incrementing the address data. [0031-0036]

As per claim 28, the combination of Andreas and Floyd disclose wherein the means for modifying the address data comprises a means for incrementing the address data. [0031-0036]

As per claim 29, the combination of Andreas and Floyd disclose wherein the means for modifying the first address data comprises a means for incrementing the first address data. [0031-0036]

As per claim 30, the combination of Andreas and Floyd disclose wherein the step of modifying the first address data in the first IC to produce first modified address data different from the first address data, comprises incrementing the first address data in the first IC to produce first modified address data different from the first address data. [0031-0036]

As per claim 31, the combination of Andreas and Floyd disclose wherein the step of modifying the first modified address data in the second IC to produce second

modified address data, comprises incrementing the first modified address data in the second IC to produce second modified address data. [0031-0036]

As per claim 32, the combination of Andreas and Floyd disclose wherein each address of the series of addresses produced by the controller on the shared bus is different. [0031-0036]

### ***Response to Amendment***

7. Applicant's amendment filed on 10/08/04 have been fully considered but does not place the application in condition for allowance.

a. In response to applicant's argument that in Andreas the slave devices are never assigned an address. Examiner respectfully disagrees. As Andreas notes at [0021-0026] discloses the communication between master 110 and devices 120-150 via sharing bus 160. The sharing bus 160 carries commands, addresses and data between the master and devices. Each command associated with specific address for specific device. In order to select a specific device the unique identification of each device must be provided by master. [0021-0026]. Thus, the prior art teaches the invention as claimed and the claims do not distinguish over the prior art as applied.

### ***Conclusion***

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. *Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kim Huynh whose telephone number is (571)272-3635 or via e-mail addressed to [kim.huynh3@uspto.gov]. The examiner can normally be reached on M-F 9.00AM- 6:00PM. The fax phone numbers for the organization where this application or proceeding is assigned are (703)872-9306 for regular communications and After Final communications.*

*Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-2100.*

Kim Huynh

Dec. 31, 2004



**TIM VO**  
**PRIMARY EXAMINER**